05 CPU

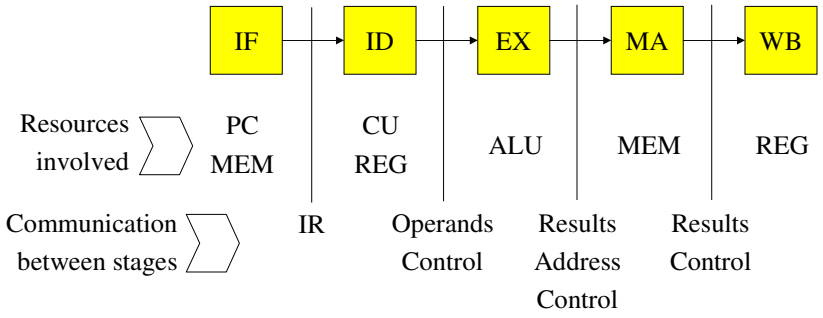
05.01 Elementary pipelining and performance metrics

- Execution steps
- Multi-cycle implementation
- Pipelining
- Performance metrics

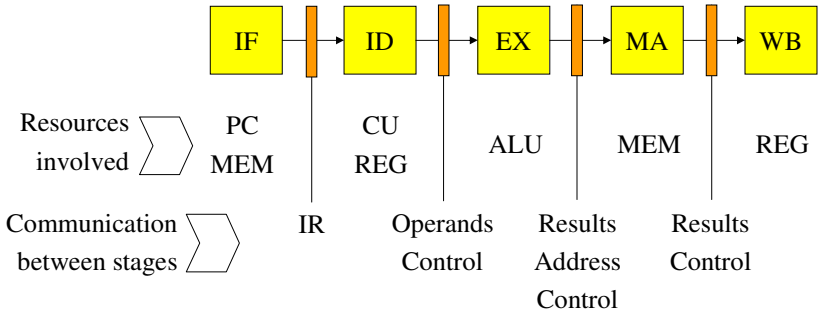
Execution steps

1. IF: Instruction fetch
   Load a new instruction from memory
2. ID: Instruction decode
   Decode the instruction and retrieve operands from registers
3. EX: Execute
   Perform computation
4. MA: Memory Access
   Read or write data in memory
5. WB: Write Back
   Write results back into the internal registers

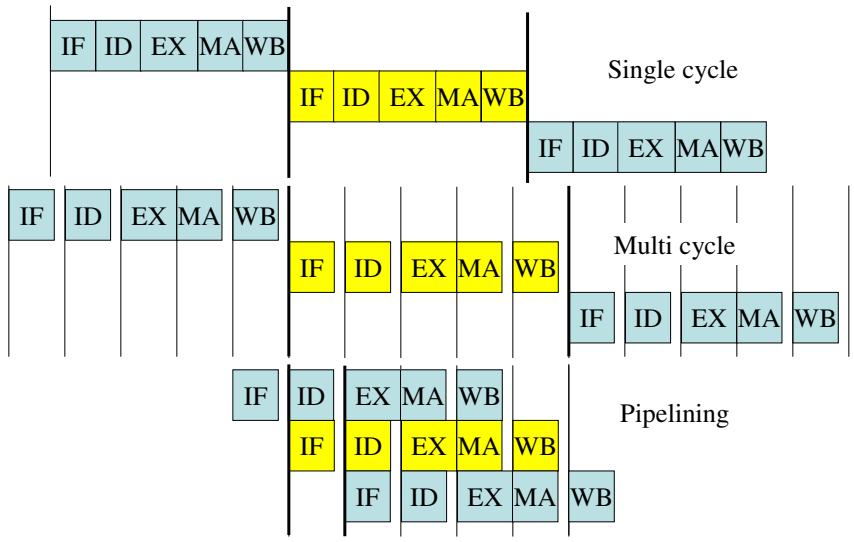
Execution steps



Multi-cycle implementation



Performance



Performance metrics

- CPUT [sec/program]
- CPUC [clocks/program]
- Tclk [sec/clock]
- CPI [clocks/instruction]
- IC [instruction/program]
- MIPS [Minstructions/sec]
- RMIPS = CPUT(ref)/CPUT*MIPS(ref)
- Latency [clocks]
- Throughput [instructions/sec]

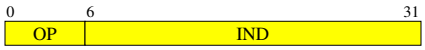
05 CPU

05.02 Reference architecture: DLX

- Minimum instruction set
- Reference architecture
- Reference architecture at work

Minimum instruction set

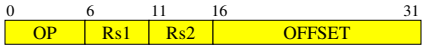
Jump instruction



(F1)

JMP label ;PC ← INDx4 000100

Conditional branch

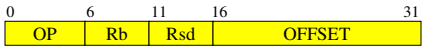


(F2)

JE R2, R3, dest ;if R2==R3 then PC ← PC+OFFSETx4 000101

JS R2, R3, dest ;if R2 < R3 then PC ← PC+OFFSETx4 000110

Memory access

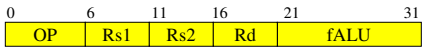


(F2)

LD R1, 100(R2) ;R1 ← M[R2+100] 000010

ST 200(R1), R2 ;M[R1+200] ← R2 000011

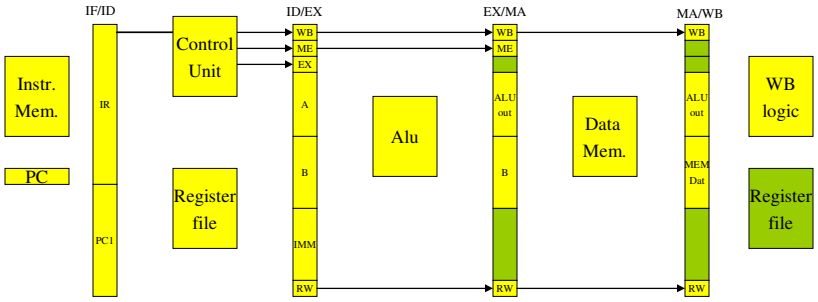
Arithmetic/Logic operations



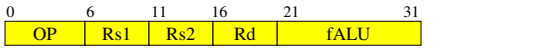
(F3)

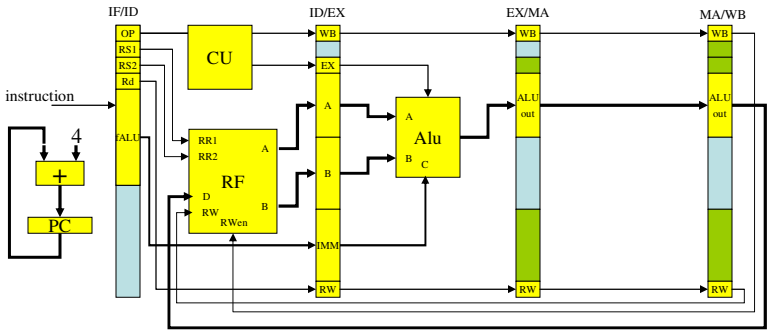
ADD R1, R2, R3 ;R1 ← R2+R3 000001

Reference architecture

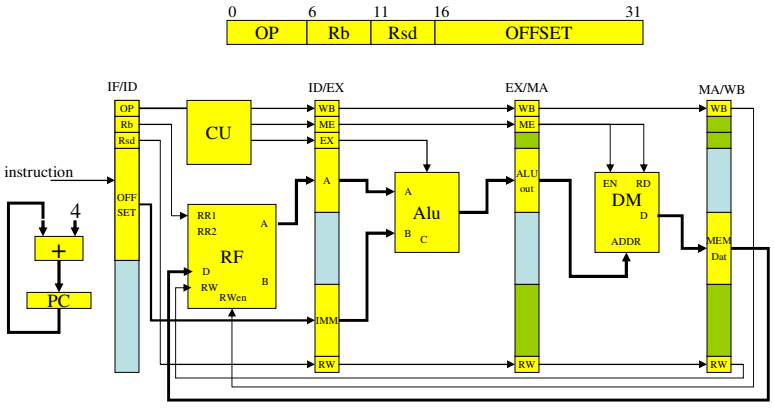


Arithmetic operations

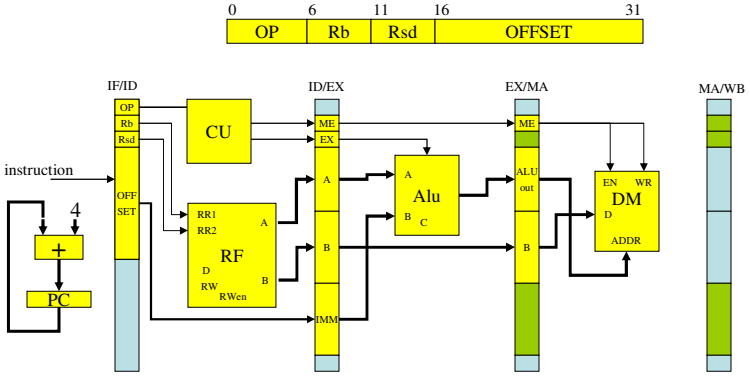




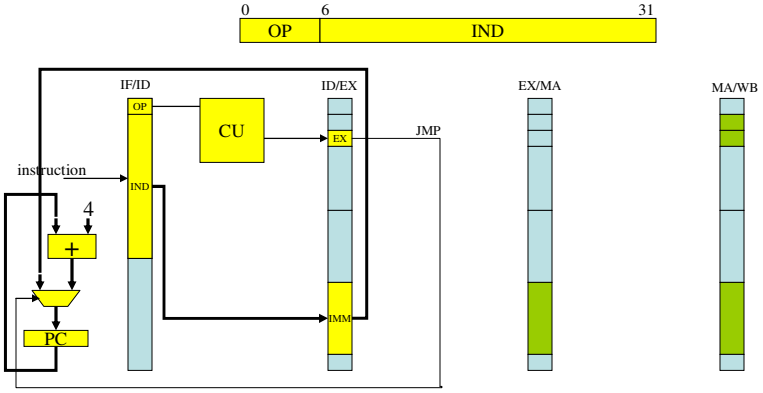
Memory accesses (LD)



Memory accesses (ST)



Unconditional branch (JMP)



Conditional branch (JS, JE)