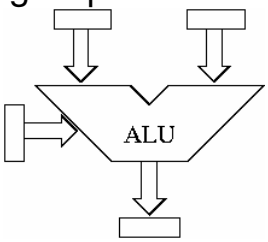
04 Computer systems

04.01 Von-Neumann bottleneck and CPU micro-architecture

- From RTL design to ALU
- Von Neumann architecture
- CPU micro-architecture
- Fetch-execute loop
- Internal communication
- Control unit design

From RTL design to ALU

- With respect to RTL design styles, the ALU can be viewed as a *shared multi-function unit that executes (sequentially) all the operations in the data path*
- Resource sharing requires steering logic and control unit

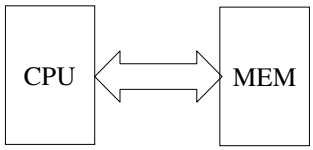


Von Neumann machine

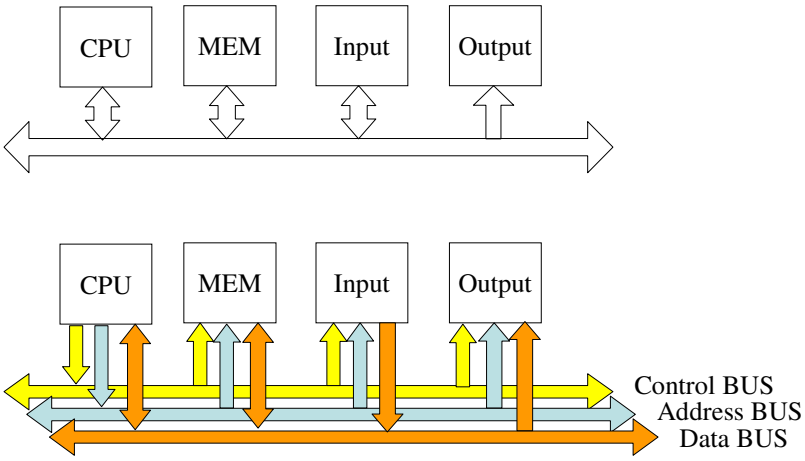
- Is a machine that reads from a memory and executes (one at the time) the instructions belonging to a finite (functionally complete) instruction set
- Any data-processing task can be performed (provided that the sequence of instructions to be executed is stored in memory) by alternating two phases:
  - Instruction *fetch*
  - Instruction *execution*
- Fetch and execution are controlled by a *control unit*

Von Neumann bottleneck

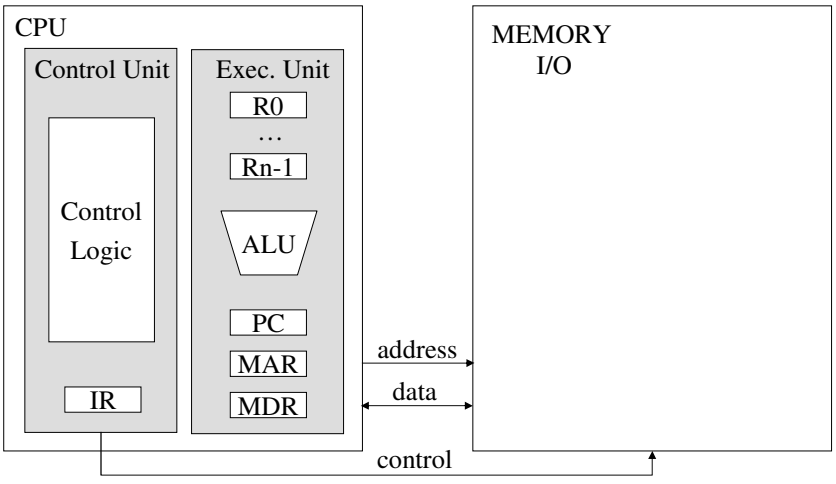
- The width of the communication channel between memory and CPU is much smaller than memory
- The communication channel is a bottleneck



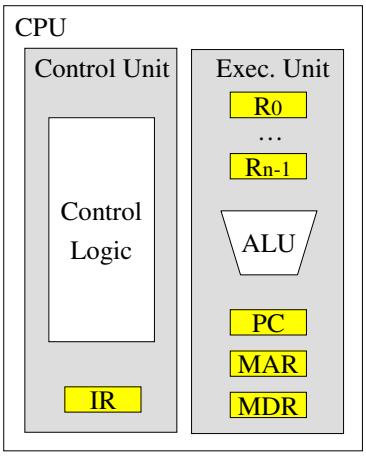
Main architectural elements



CPU microarchitecture



CPU registers



- Instruction register (IR)
- Program counter (PC)
- Memory address register (MAR)
- Memory data register (MDR)
- Generic registers $R_0 \ldots R_{n-1}$

Fetch-execution loop

1. MAR ← PC
2. MDR ← MEM[MAR]
3. IR ← MDR
4. Decode
5. PC ← PC+1
6. Execute
7. Go back to 1

1. IR ← MEM[PC]
2. Decode
3. PC ← PC+1
4. Execute
5. Go back to 1

Instruction execution

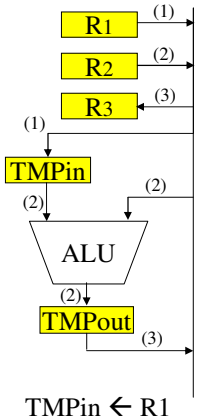
ADD R3,R1,R2 (R3 ← R1+R2)

1. Operand fetch
   Bring the operands at the inputs of ALU
2. Execute
   Compute sum
3. Write back
   Put the result in the destination register

Execution steps are controlled by the control unit, which generates the control signals for registers and MUXes

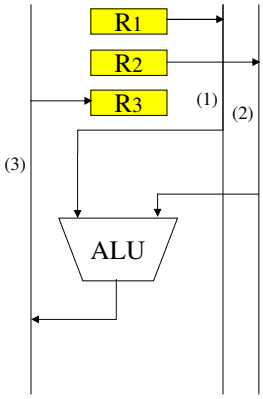
Internal communication

Single internal BUS



1. TMPin ← R1
2. TMPout ← TMPin + R2
3. R3 ← TMPout

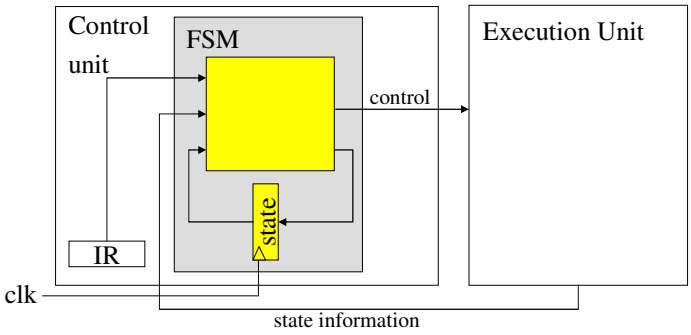
3 internal BUSes



1. R3 ← R1+R2

Control Unit Design

Random logic approach



Control Unit Design

Microprogrammed approach