03 Logic networks

03.05 Digital systems

- RTL representation
- Data path and Control unit
- Project styles
- Examples
- Data transfers among registers
- BUS and Address

Register-Transfer Level (RTL)

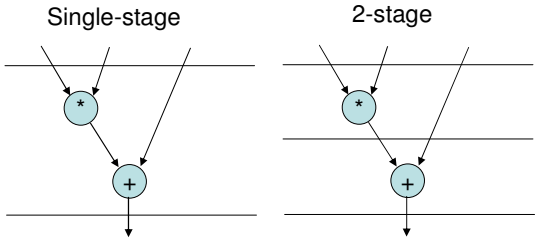
- Building blocks:
  - Registers
  - Functional macros
  - Steering logic
  - Finite state machines
- Data path
  - Functional part of the design composed of registers, functional macros and steering logic (interconnections and multiplexers)
- Control unit
  - FSM that generates the control bits for the multiplexers of the data path

Project styles

1. Single-stage network (e.g., RCAn)
   - Computation requires a single clock cycle
2. N-stage network (e.g., SRCAn)
   - Computation requires N clock cycles
   - Stages may be balanced or unbalance
3. Pipelining (e.g., PRCAn)
   - A new computation is started every clock cycle independetly of the latency
4. Resource sharing (e.g., BSAn)
   - The same functional macro is used to perform different operations in different clock cycles

Example

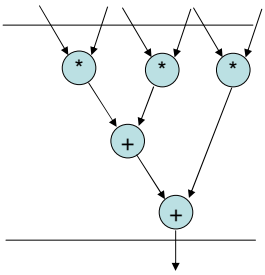
- F=a*b+c

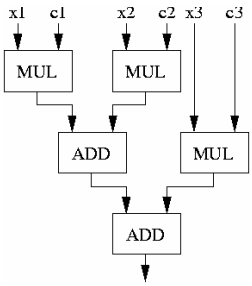


Tc=Tc(ADD)
Tp=Tp(MUL)+Tp(ADD)

Example

- F=x1*c1+x2*c2+x3*c3

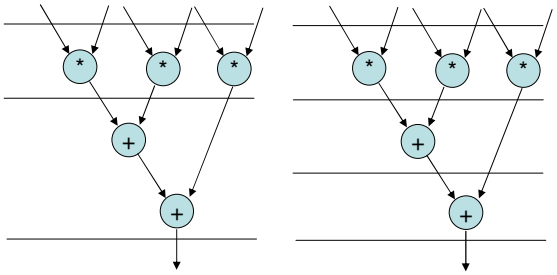


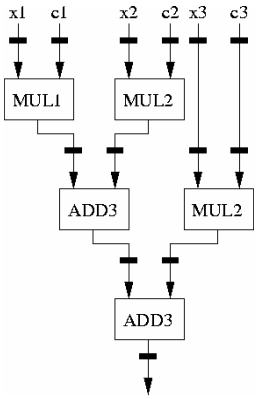


Tc=Tc(MUL)+Tc(ADD)
Tp=Tc(MUL)+2Tp(ADD)

Example

- F=x1*c1+x2*c2+x3*c3



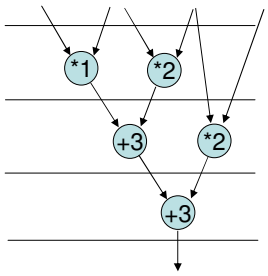


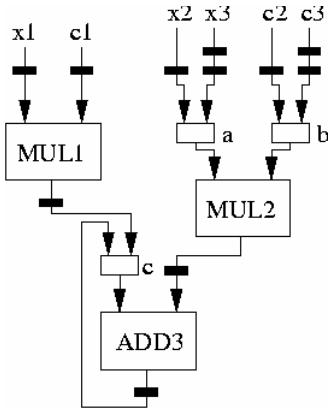
2-stage network has lower latency than
3-stage network iff Tp(ADD)<3/4 Tp(MUL)

2-stage network has higher throughput than
3-stage network iff Tp(ADD)<1/2 Tp(MUL)

Example

- F=x1*c1+x2*c2+x3*c3





Resource sharing:
Use 2 multipliers to perform 3 products
Use 1 adder to perform 2 sums

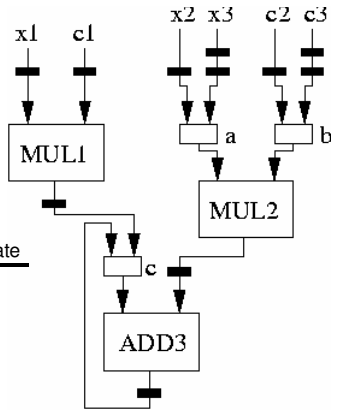
Control unit

clock cycle	a	b	c
0	0	0	--
1	1	1	1
2	--	--	0

clock cycle	a	b	c
00	0	0	--
01	1	1	1
10	--	--	0

clock cycle	control
00	0
01	1
10	0

state	control	next state
00	0	01
01	1	10
10	0	00



control = s_0
$s_0^{next} = s_0's_1'$
$s_1^{next} = s_0$

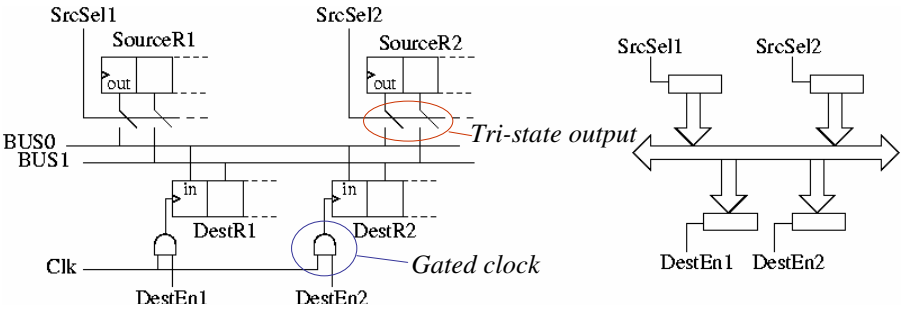
Data transfer among registers (BUS)

Shared communication channel (BUS)

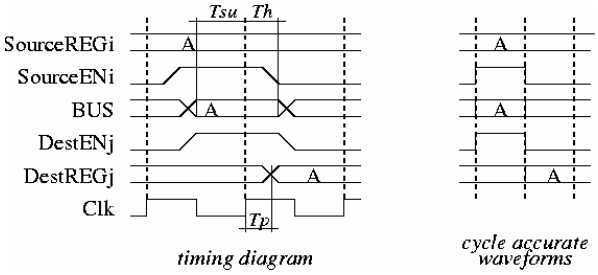
Issues:

•Select a single (*source*) register at the time to drive the BUS

•Enable a single (*destination*) register at the time to get data from the BUS



Data transfer among registers (BUS)



Addressing