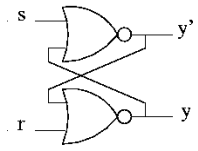
03 Logic networks

03.03 Sequential circuits

- Dealing with feedback
- Finite state machines
- Latches
- Flip flops
- Registers
- Synchronous sequential circuits

Dealing with feedback



s	r	y	y'
0	0	?	?
0	1	0	1
1	0	1	0
1	1	0	0

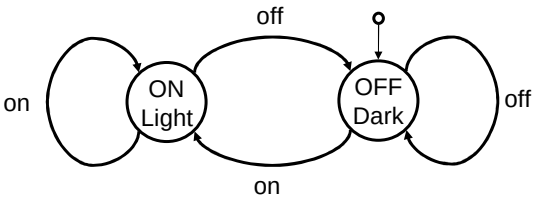
s	r	y	y'	y	y'
0	0	0	0	1	1
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1			

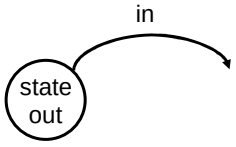
Sequential circuits: FSMs

- Finite state machines (FSM): (S,I,O,f,g,s_0)
  - *Output* function $o=f(s,i)$
  - *Next-state* function $s^{next}=g(s,i)$
  - Representation: state diagram
- Classification:
  - Combinational $f:I \rightarrow O$
  - Sequential (*Mealy*'s) $f:SxI \rightarrow O$ $g:SxI \rightarrow S$
  - Sequential (*Moore's*) $f:S \rightarrow O$ $g:SxI \rightarrow S$
- *Asynchronous vs Synchronous*

Moore's FSM: example

Case of a simple power supply system controlled by an on/off switch and monitored by a led





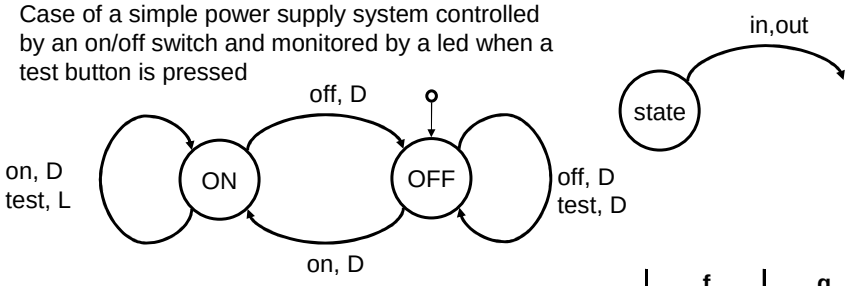
S = {ON,OFF}
I = {on,off}
O = {Light,Dark}

f: S → O
g: SxI → S

State	Input	f Output	g Snext
OFF	off	Dark	OFF
OFF	on	Dark	ON
ON	off	Light	OFF
ON	on	Light	ON

Mealy's FSM: example

Case of a simple power supply system controlled by an on/off switch and monitored by a led when a test button is pressed

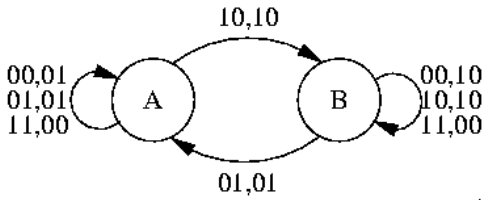


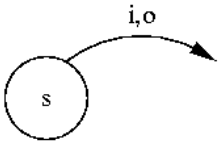
S = {ON,OFF}
I = {on,off,test}
O = {Light,Dark}

f: SxI → O
g: SxI → S

State	Input	f Output	g Snext
OFF	off	Dark	OFF
OFF	on	Dark	ON
OFF	test	Dark	OFF
ON	off	Dark	OFF
ON	on	Dark	ON
ON	test	Light	ON

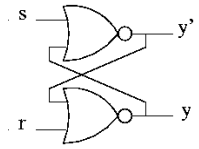
FSMs: example





state	input (sr)	f	g
A	00	01	A
A	01	01	A
A	10	10	B
A	11	00	A
B	00	10	B
B	01	01	A
B	10	10	B
B	11	00	B

Latch SR



latch SR

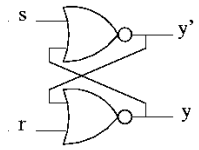
			y	y'
y'	s	r	f	g
0	0	0	**1**	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	0
1	0	0	**0**	1
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

RESET — HOLD — SET

In order to use the circuit to store a bit, we need three input configurations to:

- set y=1 regardless of the current state
- set y=0 regardless of the current state
- keep y unchanged

Latch SR



latch SR

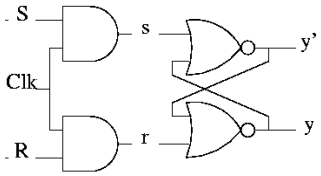
			y	y'
y'	s	r	f	g
0	0	0	**1**	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	0
1	0	0	**0**	1
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

RESET — HOLD — SET

(s,r) = (1,0) SET
(s,r) = (0,1) RESET
(s,r) = (0,0) HOLD
(s,r) = (1,1) NOT ALLOWED

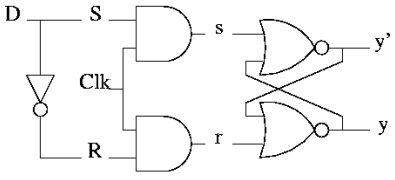
Notice that y'=NOTy for all allowed input configurations

Flip Flop SR



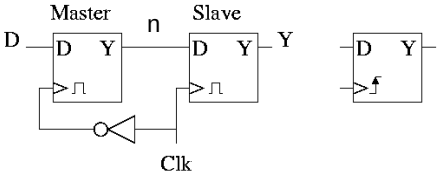
Clk	*S*	*R*	*s*	*r*	
0	0	0	0	0	HOLD
0	0	1	0	0	HOLD
0	1	0	0	0	HOLD
0	1	1	0	0	HOLD
1	0	0	0	0	HOLD
1	**0**	**1**	**0**	**1**	**RESET**
1	**1**	**0**	**1**	**0**	**SET**
1	1	1	1	1	NOT ALLOWED

Flip Flop D Level Sensitive

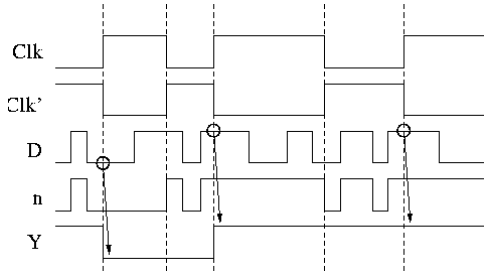


Clk	***D***	*S*	*R*	*s*	*r*	
0	0	0	1	0	0	HOLD
0	1	1	0	0	0	HOLD
1	0	**0**	**1**	**0**	**1**	**RESET**
1	1	**1**	**0**	**1**	**0**	**SET**

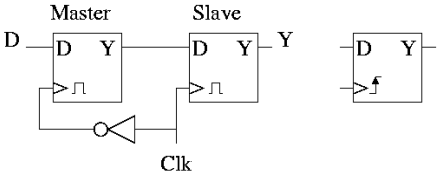
Flip Flop D Edge Triggered



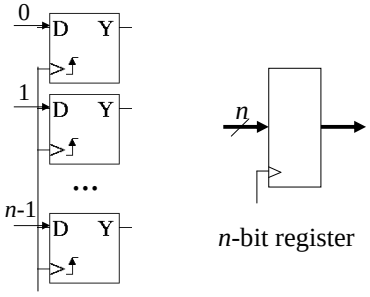
Flip Flop D edge triggered



Registers

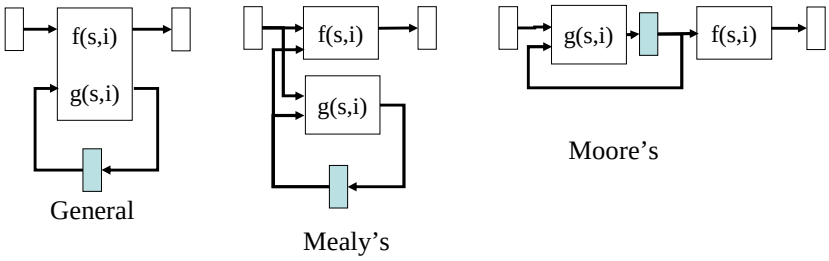


Flip Flop D edge triggered



n-bit register

Synchronous Sequential Circuits



General

Mealy's

Moore's